## R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus comprising one or more logic circuits configured to provide logical operation. The logic circuits may comprise (i) programmable logic elements and (ii) non-programmable logic elements within a programmable logic device (PLD).

## SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the specification on, for example, page 7, line 19 through page 8, line 9; and page 6, lines 9-10.

## CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-20 under 35 U.S.C. §102(b) as being anticipated by Ikawa et al. '686 (hereinafter Ikawa) has been obviated by appropriate amendment and should be withdrawn.

Ikawa discloses a semiconductor integrated circuit device (Title of Ikawa).

In contrast, claim 1 of the present invention concerns one or more logic circuits comprising (i) programmable logic elements and (ii) non-programmable logic elements within a

programmable logic device (PLD). Claim 15 (means) and claim 16 (method) provide similar limitations. Ikawa appears silent regarding a programmable logic device as presently claimed. Ikawa also appears silent regarding (i) programmable logic elements and non-programmable logic elements within the programmable logic device, as presently claimed. While the assertion that the predetermined unit digital logic circuits discussed in column 9, lines 50+ are the same as the dedicated logic as presently claimed may be accurate, the assertion does not address programmability. In particular, the present invention claims a programmable logic device having programmable elements and non-programmable elements. While Ikawa discusses a programmable interconnect, Ikawa does not disclose or suggest programmable elements. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

More specifically, Ikawa appears related to an application specific integrated circuit (ASIC), not a PLD as presently claimed. For example, Ikawa appears silent regarding programmable logic elements, which one skilled in the art would associate with a PLD. Ikawa does not disclose or suggest programmable elements, as presently claimed. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, claim 10 appears to be independently patentable over Ikawa. In particular, Ikawa does not disclose or suggest non-programmable logic elements, programmable logic elements and a routable interconnect matrix as in claim 10. Claims 2-14 and 17-21 depend, either directly or indirectly from independent claims 1 or 15 which are now believed to be allowable.

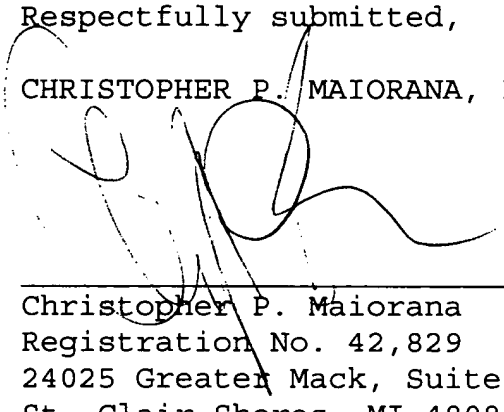
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Christopher P. Maiorana
Registration No. 42,829
24025 Greater Mack, Suite 200
St. Clair Shores, MI 48080
(586) 498-0670

Dated: March 19, 2002

Docket No.: 0325.00361